JOB OFFER

Position : PhD Student– Avalanche behaviour of multichip power SiC MOSFET modules

AXES / COMPTENCES / PROJECT	Greener Technologies / High Reliability Energy / Project SiCRET+

TYPE OF CONTRACT	☐ Secondment ☐ Permanent ☐ Fixed Term	☒ PhD Thesis ☐ Apprentice ☐ POST DOC	DURATION/DATE 36 mois Oct. 2023 • Sept. 2026

% of activity for a secondment : ……

PLACE	☒ IRT Toulouse ☐ IRT Bordeaux ☐ IRT Sophia ☒ **Other : AMPERE laboratory (Villeurbanne)**	TECHNICAL STAFF TO MEET DURING INTERVIEW	1/ Fabio COCCETTI 2/ Bernardo COGO 3/ Franck VANGRAEFSCHEPE 4/ Hervé MOREL (Thermal supervisor)

FIRM/ LABORATORY

The Saint Exupéry Technological Research Institute (IRT) is an accelerator for science, technological research and transfer to the aeronautics and space industries for the development of innovative solutions that are safe, robust, certifiable and sustainable.
We offer on our sites in Toulouse, Bordeaux, Sophia Antipolis an integrated collaborative environment made up of engineers, researchers, experts and doctoral students from industrial and academic backgrounds for research projects and R&T services backed by technological platforms around 4 areas: advanced manufacturing technologies, greener technologies, methods & tools for the development of complex systems and smart technologies.
Our developed technologies meet the needs of industry, integrating the results of academic research.
The AMPERE laboratory, based next to Lyon, has been working for years on Wide Band Gap (WBG) power components, and particularly on to assess their reliability.

MISSIONS

The thesis will benefit from a professional framework of excellence and very stimulating as it brings together the best industrial experts in the field of electrification for energy transition and the top laboratories working on power electronics and reliability. Indeed, the PhD will be integrated in the SiCRET+, collaborative project that gathers industries of aeronautics and space, railway, automotive, electrical network and academic laboratories in Toulouse, Paris, Lyon, Bordeaux in order to enhance knowledge about the reliability of SiC MOSFET power modules : understanding of failure modes, development of testing and ageing methodologies, ageing modelling, proposition of rules and good practice, especially for paralleling dice in a module.

The parallelization of chips in a module to increase the current gauge is a technique commonly used and well mastered in the case of Si chips whose behaviour, drifts during lifetime and failure modes are well known. In the case of SiC chips, knowledge is much more incomplete and there is a fear of anomalous behaviour if the chips associated in parallel have too different parameters, whether at the beginning of life or following an unbalanced aging due to a too asymmetrical design of the module. The SiCRET+ project aims to explore these issues, both for the normal use of the module (normal switching) and for abnormal but inevitable cases of life that the modules must be able to withstand (avalanche, short circuit at the load, over-current on the internal diode...).

The proposed research aims to study the behaviour of SiC chips put in parallel, both during normal switching and during abnormal avalanche-type situations, i.e. when the voltage becomes very high and is limited by the phenomenon of impact ionization. Indeed, an unbalanced thermomechanical stress between chips can lead to a different drift of the functional parameters of the chips. Similarly, during the avalanche, it is feared that chips with different parameters will not react synchronously, transferring all the constraints to a single chip.

The associated tasks are:

- Bibliography covering several topics: electro-thermal modeling of SiC MOSFETs, constraints and problems induced by the parallelization of chips (Si and SiC), definition and maturity of SOA (Safe Operating Area), aging mechanisms induced by abnormal surge events.
- Study, by simulation and testing, of the normal switching of chips put in parallel. Evaluation of the effect of parasitic elements of the module on this behaviour.

- Study, by simulation and tests, of the avalanche on chips put in parallel. Evaluation of the effect of imbalances between chips and parasitic elements of the module on this behaviour.
- Definition of a dynamic SOA taking into account avalanche behaviour.
- (Depending on the time available, an extension of the methodology may be done to include other surge-type phenomena, for example the overload of the internal diode).

DESIRED PROFILE

Bac + 5 (M2 or Engineer) in the field of electrical engineering.

Interest in the correlation between experimental and numerical data in a cooperative framework between different institutions and companies.

Preferably an experiment, in power electronics or on power components in SiC would be appreciated.

TECHNICAL KNOWLEDGE

- Knowledge of electrical materials, and/or multi-physics coupling.
- Mastery of circuit simulation software.
- Appetite in the realization of electrical or even thermal measurements.
- Notions of reliability would be a plus.
- English (written and oral): level B2 to C1.
- Writing and communication skills.

SKILLS

Teamwork / Adaptability / Rigor / Reliability (keeping commitments) / Ability to analyze and synthesize / Mobility

IF INTERESTED,

Please apply to :

franck.vangraef@irt-saintexupery.com
herve.morel@insa-lyon.fr,

This job offer is also on our website : www.irt-saintexupery.com